

## LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) The process for the manufacture of a substrate for a superjunction device, said process comprising the steps of: forming only a first epitaxial semiconductor layer of a given thickness and of a given impurity concentration of a first conductivity type atop a support body forming a plurality of spaced implants of a second conductivity type on the surface of said first epitaxial layer; forming only a second epitaxial layer of a given thickness and of a given concentration and of said first conductivity type atop said first layer; and thereafter heating said substrate and said implants to cause said implants to diffuse downwardly into said first layer and upwardly into said second layer, thereby forming spaced pedestals of said second conductivity type within said first and second layers; the total charge of each of said pedestals being approximately equal to the total charge in the volume of said first and second layers which surrounds said pedestals, wherein said first epitaxial semiconductor layer and said second epitaxial semiconductor layer together form a single epitaxial layer, and wherein said pedestals are formed near a control region of said single epitaxial layer spaced from said support body.
2. (Original) The process of claim 1, in which said first and second layers are silicon.
3. (Original) The process of claim 1, wherein said first and second layers are of the same thickness and impurity concentration.
4. (Original) The process of claim 2, wherein said support body is a silicon wafer.
5. (Original) The process of claim 4, wherein said first and second layers are of the same thickness and concentration.

6. (Original) The process of claim 4, wherein said silicon wafer has the same conductivity type as said first and second layers.

7. (Currently Amended) The process for the manufacture of a superjunction device comprising the steps of: forming only a first epitaxial semiconductor layer of a given thickness and of a given impurity concentration of a first conductivity type atop a support body; forming a plurality of spaced implants of a second conductivity type on the surface of said first epitaxial layer; forming only a second epitaxial layer of a given thickness and of a given concentration and of said first concentration type atop said first layer; heating said substrate and said implants to cause said implants to diffuse downwardly into said first layer and upwardly into said second layer, thereby forming spaced pedestals of said second conductivity type within said first and second layers; the total charge of each of said pedestals being approximately equal to the total charge of the volume of said first and second layers which surrounds said pedestals; and thereafter forming MOSgated cell elements atop each of said pedestals wherein said first epitaxial semiconductor layer and said second epitaxial semiconductor layer together form a single epitaxial layer, and wherein said pedestals are formed in a central region of said single epitaxial layer spaced from said support body.

8. (Original) The process of claim 7, which further includes forming a drain electrode on the bottom of said support layer, and separating said support layer and said MOSgated cell elements into separate unitary elements.

9. (Original) The process of claim 7, wherein said support body is a silicon wafer.

10. (Original) The process of claim 9, wherein said silicon wafer has the same conductivity type as said first and second layers.

11.-17. Canceled